Reconsideration of the application is requested.

Claims 1-3 and 5-23 are now in the application. Claims 1-3 and 5-23 are

subject to examination. Claims 1, 3, 7, 8, 11, and 13 have been amended.

Claims 21, 22, and 23 have been added. Claim 4 has been canceled to

facilitate prosecution of the instant application.

Under the heading "Claim Rejections – 35 USC § 103" on page 2 of the above-

identified Office Action, claims 1-6, 8, 11-15, 18, and 20 have been rejected as

being obvious over U.S. Patent No. 4,405,980 to Hess in view of U.S. Patent

No. 5,150,471 to Tipon et al. under 35 U.S.C. § 103. Applicant respectfully

traverses, in part.

Claims 1 and 11 have been amended to include the limitations of now-

cancelled claim 4.

Claim 1 now includes a step of providing the arithmetic computation rule for

computing the plurality of addresses in the table memory as an incrementation

rule or a decrementation rule.

Claim 11 includes a hardware address computation circuit for, taking the base

address as a starting point, applying an arithmetic computation rule to produce

a plurality of addresses used by the digital processor to consecutively access

said table memory; said arithmetic computation rule being an incrementation

rule or a decrementation rule.

The prior art does not teach or suggest computing the plurality of addresses in

the table memory as an incrementation rule or a decrementation rule.

The Examiner has equated the claimed table memory with the main memory

AKU taught by Hess. The addresses of the AKU are calculated by an address

processor AR. Importantly, Hess merely teaches that the address processor

AR processes the addresses read from an address memory ASP (Please see

column 2, lines 6-9 and column 6, lines 39-43). Hess does not teach or

suggest that the address processor AR performs an incrementation rule or a

decrementation rule.

The Examiner has referenced column 2, lines 25-40 of Hess, however, upon a

closer inspection of that portion of the teaching, it is seen that the referenced

portion of the teaching relates to outputting operation commands from a

<u>program memory PS</u><sub>P</sub> to a processor ALU. The referenced portion does not

teach calculating the addresses of the main memory AKU. Therefore, applicant

respectfully believes it is clear that the cited passage does not support the

Examiner's assertions. The invention as defined by claims 1 and 11 are not

suggested by the prior art.

Claim 3 has been amended to define a step of prescribing the plurality of base

addresses unalterably in hardware, wherein the plurality of base addresses

cannot be processed by the digital processor.

Claim 22 has been added to specify that the plurality of base addresses cannot

be processed by said processor.

Support for the additions can be found by referring to the specification at page

7, lines 11-14, for example.

The Examiner has alleged that the base address register 32 shown in Fig. 1 of

Tipon et al. is hard-wired. Tipon et al., however, teach that a processor 12

loads the base address register 32, and that the loading is performed according

to a predetermined computer program (Please see column 3, lines 22-29). It

should be clear that Tipon et al. do not teach or suggest the limitations defined

by claim 3 or 22.

Claims 7 and 8 have been amended to define a Viterbi decoder hardware

arithmetic-logic unit.

Support for the addition can be found by referring to the specification at page 4,

lines 22-26.

Neither Hess nor Tipon et al. teach any method steps implementing a Vitebi

algorithm. It should therefore be clear that the cited prior art does not teach or

suggest a Viterbi decoder hardware arithmetic-logic unit.

Claim 21 has been added to define a hardware counter implementing said

arithmetic computation rule as an incrementation rule or a decrementation rule.

Claim 23 has been added to specify that the step of providing the arithmetic

computation rule is performed by providing a hardware counter that implements

the incrementation rule or the decrementation rule.

Support for added claims 21 and 23 can be found by referring to the

specification at page 16, line 14 through page 17, line 8 with reference to Fig.

2, for example.

As discussed above, Hess does not teach or suggest that the address

processor AR performs an incrementation rule or a decrementation rule.

Under the heading "Claim Rejections – 35 USC § 103" on page 6 of the above-

identified Office Action, claim 7 has been rejected as being obvious over U.S.

Patent No. 4,405,980 to Hess in view of U.S. Patent No. 5,150,471 to Tipon et

al. and further in view of U.S. Patent No. 3,833,888 to Stafford et al. under 35

U.S.C. § 103.

Even if Stafford et al. does teach the subject matter that the Examiner has

alleged and even if it would have been obvious to combine the teachings of the

references, the invention as defined by claim 7 would not have been obtained

for the reasons specified above with regard to claim 1 and the deficiencies in

the teachings of Hess and Tipon et al.

Under the heading "Claim Rejections – 35 USC § 103" on page 7 of the above-

identified Office Action, claim 19 has been rejected as being obvious over U.S.

Patent No. 4,405,980 to Hess in view of U.S. Patent No. 5,150,471 to Tipon et

al. and further in view of U.S. Patent No. 5,311,523 to Serizawa et al. under 35

U.S.C. § 103.

Even if Serizawa et al. does teach the subject matter that the Examiner has

alleged and even if it would have been obvious to combine the teachings of the

references, the invention as defined by claim 19 would not have been obtained

for the reasons specified above with regard to claim 11 and the deficiencies in

the teachings of Hess and Tipon et al.

It is accordingly believed to be clear that none of the references, whether taken

alone or in any combination, either show or suggest the features of claims 1 or

11. Claims 1 and 11 are, therefore, believed to be patentable over the art. The

dependent claims are believed to be patentable as well because they all are

ultimately dependent on claims 1 or 11.

Finally, applicant(s) appreciatively acknowledge(s) the Examiner's statement

that claims 9, 10, 16, and 17 "would be allowable if rewritten in independent

form including all of the limitations of the base claim and any intervening

claims." In light of the above, applicants respectfully believe that rewriting of

claims9, 10, 16, and 17 is unnecessary at this time.

In view of the foregoing, reconsideration and allowance of claims 1-3 and 5-23

are solicited.

In the event the Examiner should still find any of the claims to be unpatentable,

counsel would appreciate receiving a telephone call so that, if possible,

patentable language can be worked out.

A fee in the amount of \$100.00 has been enclosed for presenting two claims in

excess of twenty. Please note that claim 4 has been cancelled so there are

only 22 claims in the application.

Please charge any other fees that might be due with respect to Sections 1.16

and 1.17 to the Deposit Account of Lerner Greenberg Stemer LLP, No. 12-

1099.

Appl. No. 10/730,619 Amdt. Dated December 31, 2007 Reply to Office Action of October 10, 2007

## Respectfully submitted,

/Laurence A. Greenberg/ Laurence A. Greenberg (Reg. No. 29,308)

MPW:cgm

December 31, 2007

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